

NUP4202W1

Low Capacitance SC-88 Diode-TVS Array for High Speed Data Lines Protection

The NUP4202W1 transient voltage suppressor is designed to protect high speed data lines from ESD, EFT, and lightning.

Features:

- Low Capacitance (3 pF Maximum Between I/O Lines)
- ESD Rating of Class 3B (Exceeding 8 kV) per Human Body model and Class C (Exceeding 400 V) per Machine Model
- Protection for the Following IEC Standards:
 - IEC 61000-4-2 (ESD) 15 kV (air) 8 kV (contact)
 - IEC 61000-4-4 (EFT) 40 A (5/50 ns)
 - IEC 61000-4-5 (Lightning) 23 A (8/20 μ s)
- UL Flammability Rating of 94 V-0
- This is a Pb-Free Device

Typical Applications:

- High Speed Communication Line Protection
- USB 1.1 and 2.0 Power and Data Line Protection
- Digital Video Interface (DVI) and HDMI
- Monitors and Flat Panel Displays
- MP3

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

| Rating | Symbol | Value | Unit |
|--|-----------|--------------------------------|------------------|
| Peak Power Dissipation 8 x 20 μ S @ $T_A = 25^\circ\text{C}$ (Note 1) | P_{pk} | 500 | W |
| Operating Junction Temperature Range | T_J | -40 to +125 | $^\circ\text{C}$ |
| Storage Temperature Range | T_{stg} | -55 to +150 | $^\circ\text{C}$ |
| Lead Solder Temperature – Maximum (10 Seconds) | T_L | 260 | $^\circ\text{C}$ |
| Human Body Model (HBM) Machine Model (MM) IEC 61000-4-2 Air (ESD) IEC 61000-4-2 Contact (ESD) | ESD | 16000 400 20000 20000 | V |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Nonrepetitive current pulse per Figure 1 (Pin 5 to Pin 2)

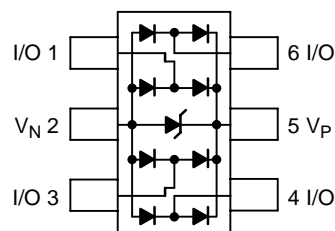


ON Semiconductor®

<http://onsemi.com>

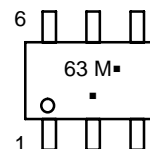
SC-88 LOW CAPACITANCE DIODE TVS ARRAY 500 WATTS PEAK POWER 6 VOLTS

PIN CONFIGURATION AND SCHEMATIC



SC-88
CASE 419B
PLASTIC

MARKING DIAGRAM



63 = Specific Device Code
M = Date Code

▪ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

| Device | Package | Shipping |
|--------------|--------------------|------------------|
| NUP4202W1T2G | SC-88 (Pb-Free) | 3000/Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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ELECTRICAL CHARACTERISTICS ($T_J=25^\circ\text{C}$ unless otherwise specified)

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|----------------------------|-----------|--|-----|-----|------|---------------|
| Reverse Working Voltage | V_{RWM} | (Note 2) | | | 5.0 | V |
| Breakdown Voltage | V_{BR} | $I_T = 1 \text{ mA}$, (Note 3) | 6.0 | | | V |
| Reverse Leakage Current | I_R | $V_{RWM} = 5 \text{ V}$ | | | 5.0 | μA |
| Clamping Voltage | V_C | $I_{PP} = 5 \text{ A}$ (Note 4) | | 8.5 | 12.5 | V |
| Clamping Voltage | V_C | $I_{PP} = 8 \text{ A}$ (Note 4) | | 8.9 | 20 | V |
| Maximum Peak Pulse Current | I_{PP} | 8x20 μs Waveform | | | 28 | A |
| Junction Capacitance | C_J | $V_R = 0 \text{ V}$, $f = 1 \text{ MHz}$ between I/O Pins and GND | | 3.0 | 5.0 | pF |
| Junction Capacitance | C_J | $V_R = 0 \text{ V}$, $f = 1 \text{ MHz}$ between I/O Pins | | 1.5 | 3.0 | pF |

- TVS devices are normally selected according to the working peak reverse voltage (V_{RWM}), which should be equal or greater than the DC or continuous peak operating voltage.
- V_{BR} is measured at pulse test current I_T .
- Nonrepetitive current pulse per Figure 1 (Pin 5 to Pin 2)

TYPICAL PERFORMANCE CURVES

($T_J = 25^\circ\text{C}$ unless otherwise noted)

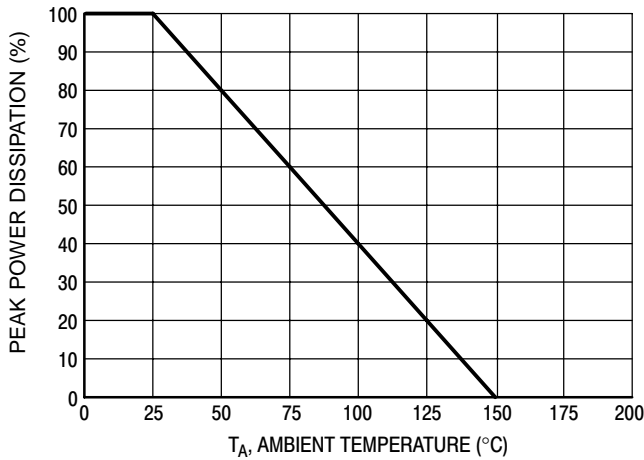


Figure 1. Pulse Derating Curve

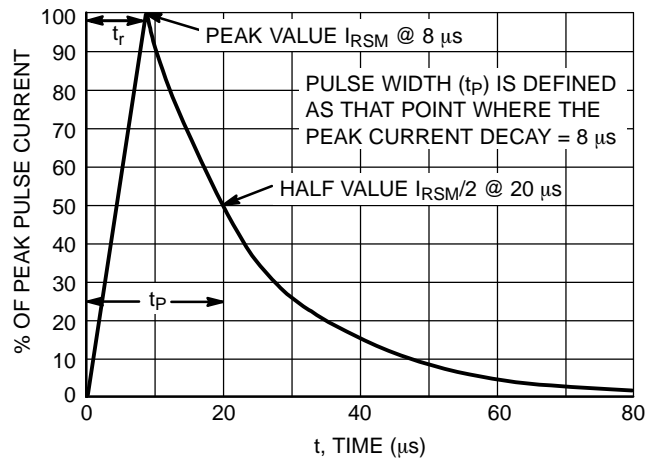


Figure 2. 8 x 20 μs Pulse Waveform

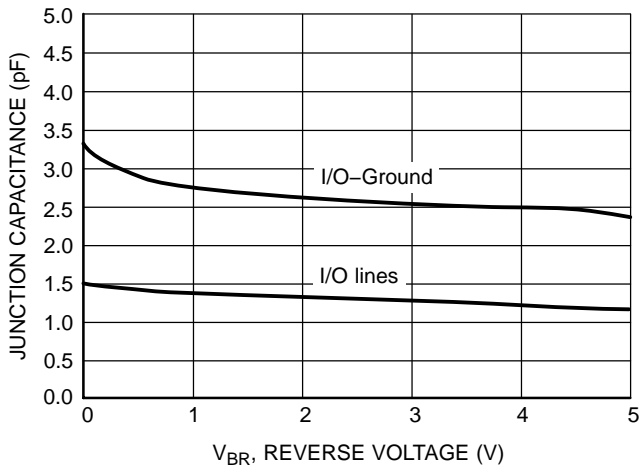


Figure 3. Junction Capacitance vs Reverse Voltage

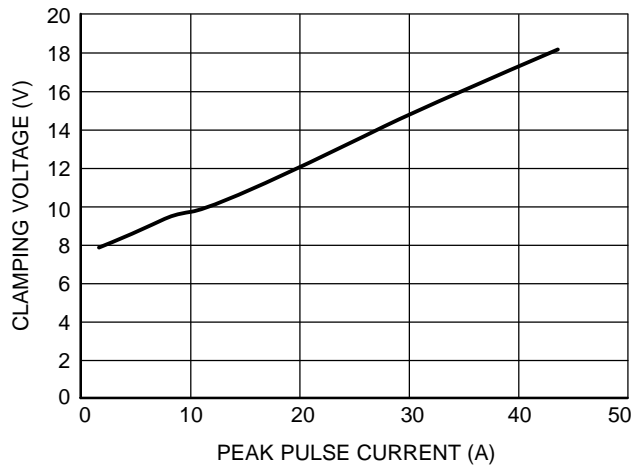


Figure 4. Clamping Voltage vs. Peak Pulse Current (8 x 20 μs Waveform)

NUP4202W1

APPLICATIONS INFORMATION

The new NUP4202W1 is a low capacitance TVS diode array designed to protect sensitive electronics such as communications systems, computers, and computer peripherals against damage due to ESD events or transient overvoltage conditions. Because of its low capacitance, it can be used in high speed I/O data lines. The integrated design of the NUP4202W1 offers surge rated, low capacitance steering diodes and a TVS diode integrated in a single package (SC-88). If a transient condition occurs, the steering diodes will drive the transient to the positive rail of the power supply or to ground. The TVS device protects the power line against overvoltage conditions to avoid damage to the power supply and any downstream components.

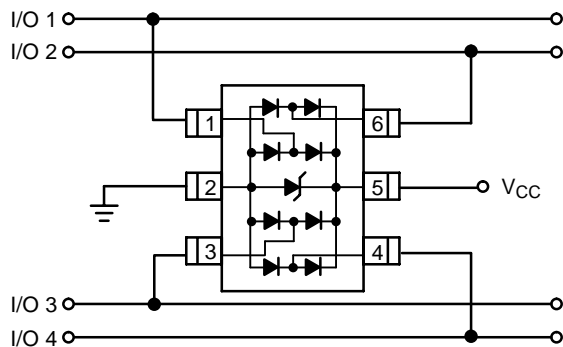
NUP4202W1 Configuration Options

The NUP4202W1 is able to protect up to four data lines against transient overvoltage conditions by driving them to a fixed reference point for clamping purposes. The steering diodes will be forward biased whenever the voltage on the protected line exceeds the reference voltage (V_f or $V_{CC}+V_f$). The diodes will force the transient current to bypass the sensitive circuit.

Data lines are connected at pins 1, 3, 4 and 6. The negative reference is connected at pin 2. This pin must be connected directly to ground by using a ground plane to minimize the PCB's ground inductance. It is very important to reduce the PCB trace lengths as much as possible to minimize parasitic inductances.

Option 1

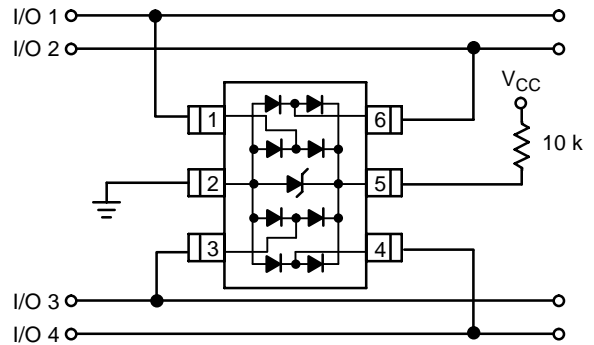
Protection of four data lines and the power supply using V_{CC} as reference.



For this configuration, connect pin 5 directly to the positive supply rail (V_{CC}), the data lines are referenced to the supply voltage. The internal TVS diode prevents overvoltage on the supply rail. Biasing of the steering diodes reduces their capacitance.

Option 2

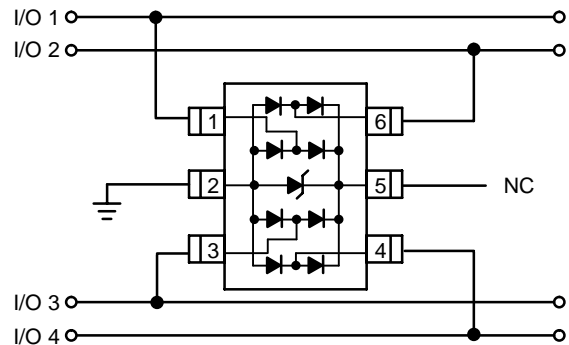
Protection of four data lines with bias and power supply isolation resistor.



The NUP4202W1 can be isolated from the power supply by connecting a series resistor between pin 5 and V_{CC} . A 10 kΩ resistor is recommended for this application. This will maintain a bias on the internal TVS and steering diodes, reducing their capacitance.

Option 3

Protection of four data lines using the internal TVS diode as reference.

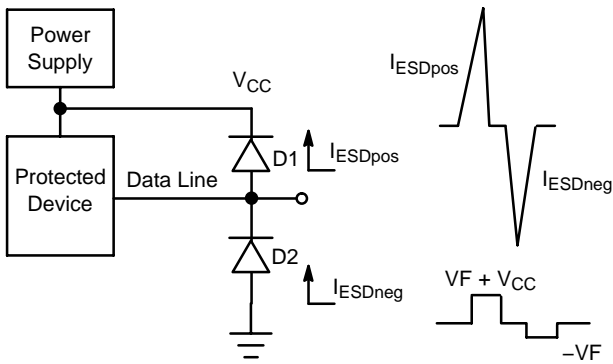


In applications lacking a positive supply reference or those cases in which a fully isolated power supply is required, the internal TVS can be used as the reference. For these applications, pin 5 is not connected. In this configuration, the steering diodes will conduct whenever the voltage on the protected line exceeds the working voltage of the TVS plus one diode drop ($V_c = V_f + V_{TVS}$).

ESD Protection of Power Supply Lines

When using diodes for data line protection, referencing to a supply rail provides advantages. Biasing the diodes reduces their capacitance and minimizes signal distortion. Implementing this topology with discrete devices does have disadvantages. This configuration is shown below:

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Looking at the figure above, it can be seen that when a positive ESD condition occurs, diode D1 will be forward biased while diode D2 will be forward biased when a negative ESD condition occurs. For slower transient conditions, this system may be approximated as follows:

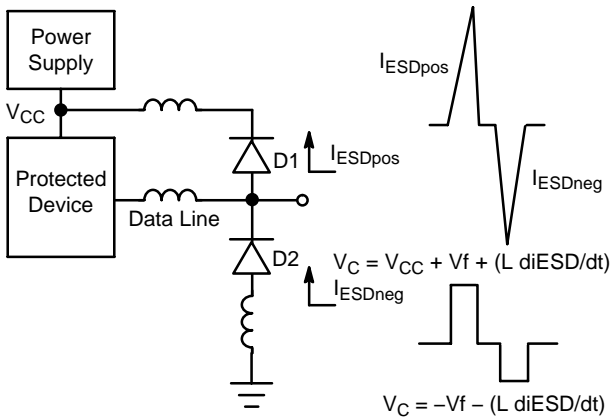
For positive pulse conditions:

$$V_c = V_{CC} + V_{fD1}$$

For negative pulse conditions:

$$V_c = -V_{fD2}$$

ESD events can have rise times on the order of some number of nanoseconds. Under these conditions, the effect of parasitic inductance must be considered. A pictorial representation of this is shown below.



An approximation of the clamping voltage for these fast transients would be:

For positive pulse conditions:

$$V_c = V_{CC} + V_f + (L \frac{di_{ESD}}{dt})$$

For negative pulse conditions:

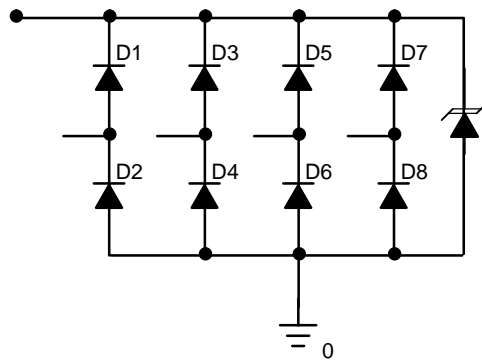
$$V_c = -V_f - (L \frac{di_{ESD}}{dt})$$

As shown in the formulas, the clamping voltage (V_c) not only depends on the V_f of the steering diodes but also on the $L \frac{di_{ESD}}{dt}$ factor. A relatively small trace inductance can result in hundreds of volts appearing on the supply rail. This endangers both the power supply and anything attached to that rail. This highlights the importance of good board layout. Taking care to minimize the effects of parasitic

inductance will provide significant benefits in transient immunity.

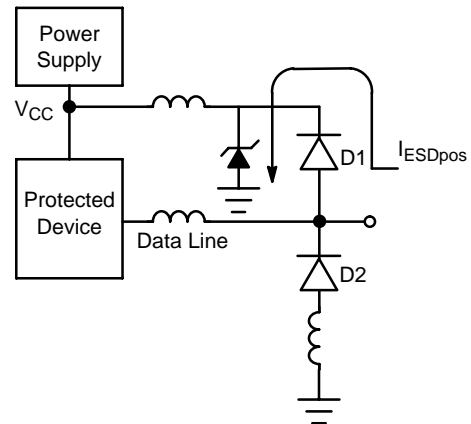
Even with good board layout, some disadvantages are still present when discrete diodes are used to suppress ESD events across datalines and the supply rail. Discrete diodes with good transient power capability will have larger die and therefore higher capacitance. This capacitance becomes problematic as transmission frequencies increase. Reducing capacitance generally requires reducing die size. These small die will have higher forward voltage characteristics at typical ESD transient current levels. This voltage combined with the smaller die can result in device failure.

The ON Semiconductor NUP4202W1 was developed to overcome the disadvantages encountered when using discrete diodes for ESD protection. This device integrates a TVS diode within a network of steering diodes.



NUP4202W1 Equivalent Circuit

During an ESD condition, the ESD current will be driven to ground through the TVS diode as shown below.



The resulting clamping voltage on the protected IC will be:

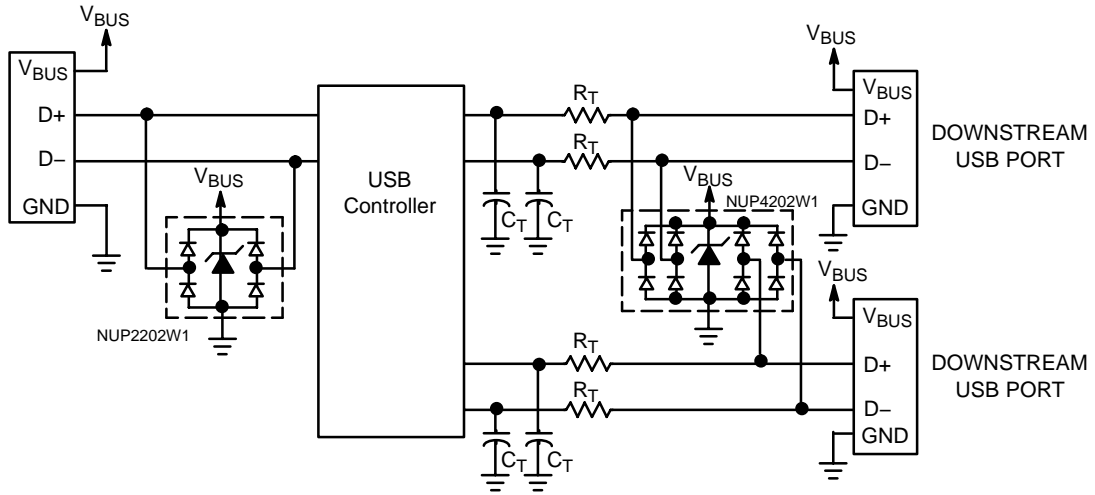
$$V_c = V_f + V_{TVS}$$

The clamping voltage of the TVS diode is provided in Figure 4 and depends on the magnitude of the ESD current. The steering diodes are fast switching devices with unique forward voltage and low capacitance characteristics.

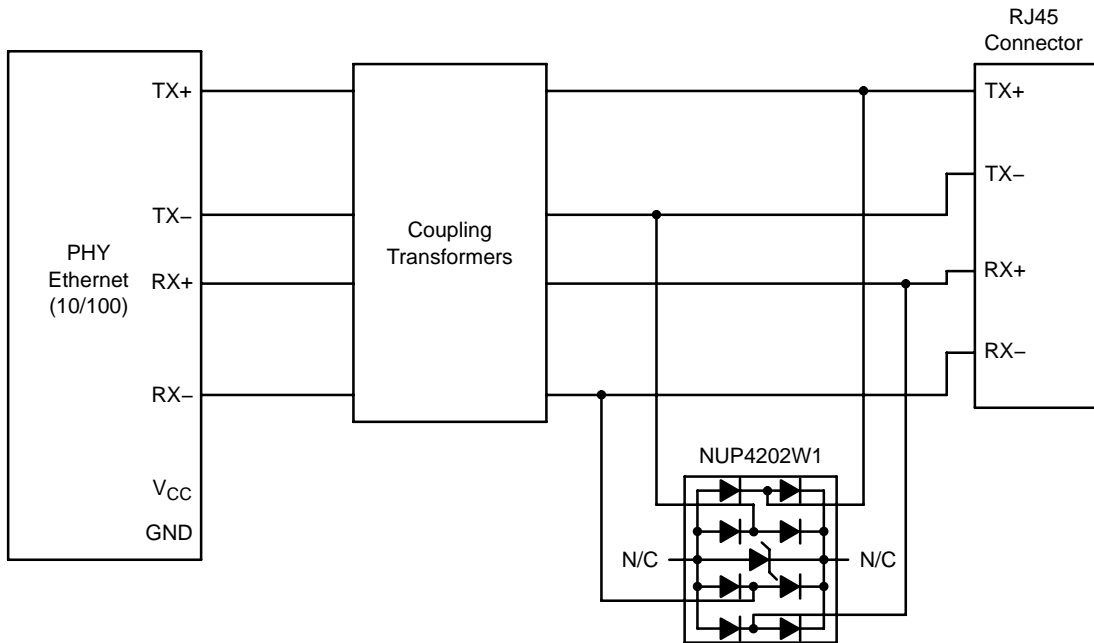
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TYPICAL APPLICATIONS

UPSTREAM
USB PORT

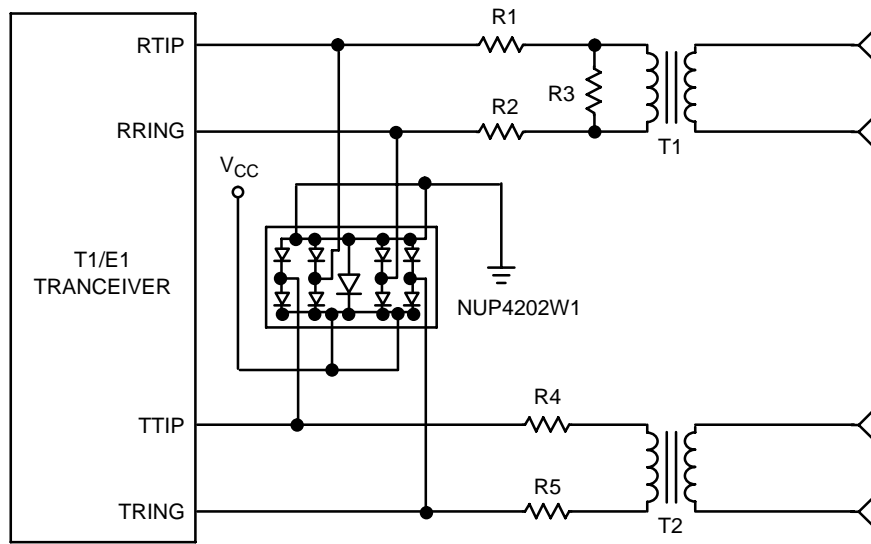


ESD Protection for USB Port



Protection for Ethernet 10/100 (Differential mode)

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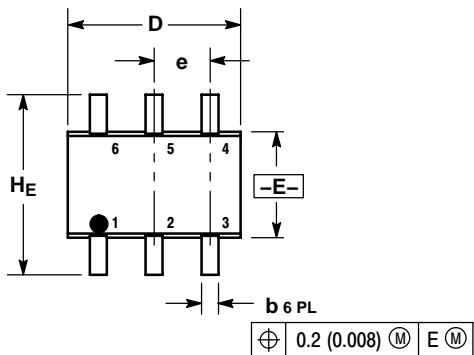
T1/E1 Interface Protection

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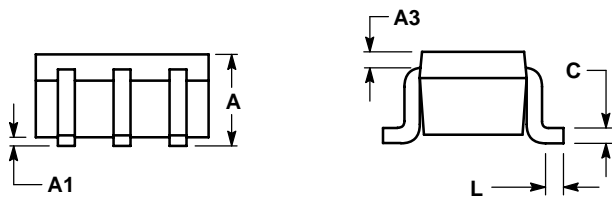
PACKAGE DIMENSIONS

SC-88/SC70-6/SOT-363
CASE 419B-02
ISSUE V

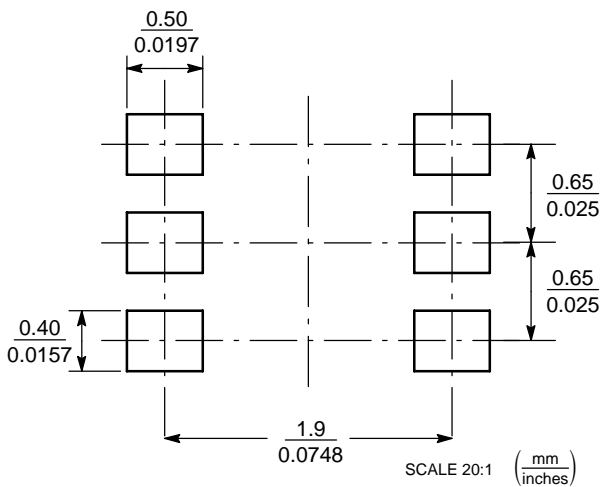
- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419B-01 OBSOLETE, NEW STANDARD 419B-02.



| DIM | MILLIMETERS | | | INCHES | | |
|-----|-------------|------|------|-----------|-------|-------|
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | 0.80 | 0.95 | 1.10 | 0.031 | 0.037 | 0.043 |
| A1 | 0.00 | 0.05 | 0.10 | 0.000 | 0.002 | 0.004 |
| A3 | 0.20 REF | | | 0.008 REF | | |
| b | 0.10 | 0.21 | 0.30 | 0.004 | 0.008 | 0.012 |
| C | 0.10 | 0.14 | 0.25 | 0.004 | 0.005 | 0.010 |
| D | 1.80 | 2.00 | 2.20 | 0.070 | 0.078 | 0.086 |
| E | 1.15 | 1.25 | 1.35 | 0.045 | 0.049 | 0.053 |
| e | 0.65 BSC | | | 0.026 BSC | | |
| L | 0.10 | 0.20 | 0.30 | 0.004 | 0.008 | 0.012 |
| HE | 2.00 | 2.10 | 2.20 | 0.078 | 0.082 | 0.086 |



SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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